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CODEN: IAASCA **ORIGINAL ARTICLE**

A Low Power Delay Product SEU tolerant ISO-DICE latch circuit design

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ABSTRACT
Soft-error interference is a crucial design challenge in the advanced CMOS VLSI circuit designs. In this paper, we proposed a SEU Isolating DICE latch (Iso-DICE) design by combing the new proposed soft-error isolating technique and the inter-latching technique used in the DICE design. To further enhance SEU-tolerance of DICE design, we keep the storage node pairs having the ability to recover the SEU fault occurring in each other pair but also avoid the storage node to be affected by each other. To mitigate the interference effect between dual storage node pairs, we use the isolation mechanism to resist high energy particle strikes instead of the original interlocking design method.Through isolating the output nodes and the internal circuit nodes, the Iso-DICE latch can possess more superior SEU-tolerance as compared with the DICE design. As compared with the FERST design which performs with the same superior SEU-tolerance, the proposed Iso- DICE latch consumes 50% less power with only 45% of power delay product in TSMC 90 nm CMOS technology.
Keyword: Soft error,Single event upset, Isolating, DICE,Latch

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INTRODUCTION

With the progress of semiconductor process, digital circuits are becoming more susceptible to noise due to reduced working supply voltage and increased transistor density.

In the advanced VLSI environment, the circuits are more easily affected by alpha particles, cosmic rays, and heat particles to cause errors, which are all summarized as soft errors [3–8].Soft errors can be categorized into two classes according to the different locations of occurrence: (1) single event transients (SETs) which occur in combinational circuits, and (2) single event upsets (SEUs) which occur in storage elements, latches, or register nodes when the logic state of circuits changes undesirably. Therefore, most recent researches focus on devising robust schemes for latches. In this paper, we will further present a robust latch design that not only performs with superior soft-error resistant capability but also with lower power delay product (PDP).

In the existing literature designs, a variety of methods have been used to increase the SEU tolerance capability of latch circuits, such as: (1) interlock circuits with a redundant feedback path, such as Dual Interlocked Storage Cell (DICE) [1]; (2) strengthening equivalent capacitance for those internal nodes which have low critical charge, such as Schmitt Trigger latch (ST) [11]; (3) increasing the number of nodes to have the same electrical potential, such as SEU-A design [12]; (4) latches capable of filtering and masking SEUs, such as feedback redundant SEU-tolerant latch (FERST) [2]; and (5) constructing redundancy circuits together with a voting circuit to determine the valid output, such as Triple-Modular Redundancy (TMR) [13–15]. Among these SEU-tolerant approaches, DICE design can provide good SEU tolerance with less hardware cost and FERST design
can provide even superior SEU-tolerance. TMR can also provide superior and nearly perfect SEU-tolerance; however, it is always
criticized for its hardware complexity since it requires three times the circuit area. Therefore, in this paper we proposed a new SEU tolerant latch that can provide superior SEU-tolerance as FERST latch but with much lower PDP.

Our proposed design is based on DICE architecture because of its advantages of simplicity. To further enhance the SEU-tolerance of DICE latch, we proposed an isolating technique which is capable of masking soft-error between DICE circuit's internal and output nodes. The proposed Iso-DICE latch can have both the DICE latch's capability of masking SEUs by cross-coupled inter-latching and the FERST latch circuit's isolation concept of having more than two storage points. Therefore, the Iso-DICE latch can have a higher

SEU tolerance with a smaller power-delay-product while efficiently preventing output nodes from being affected by the SEU in the internal nodes of latch circuit.

PREVIOUS WORKS

Fig 1 shows a convectional latch with a feedback path to keep the stored logic value. The feed forward signal transmission path is constructed of one transmission gate and two inverters. The storage feedback path is constructed of one transmission gate andone inverter. When theclk signal is '1', TG1 turns on and TG2 turns off. The input value is directly propagated from D to Q. When the clk signal is '0', TG1 turns off and TG2 turns on. Thus, the storage logic state is kept unperturbed. However, when the circuit is in latching mode, transient voltage caused by unexpected ionizing particles with high energy may cause a SEU. The internal node in 1 has the minimum critical charge and is the node most
likely to flip. The advantage of this latch is its simplicity. However, the drawback is that it is highly susceptible to SEU.

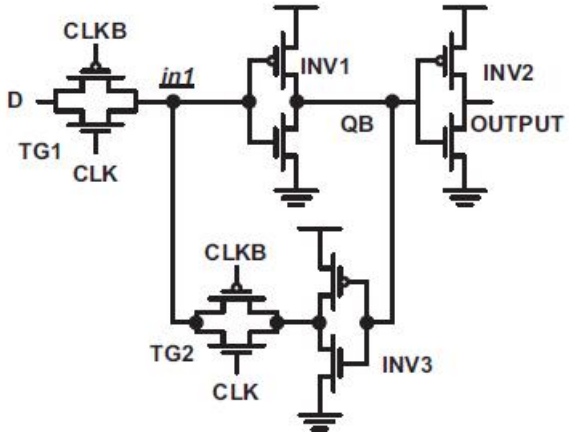

Fig1.Conventional Latch

The DICE latch [1] is a well-known SEU-tolerant design because of its superior soft-error tolerance ability. When compared with other existing SEU-tolerant latch circuits for the weakest internal nodes, the DICE latch has a relatively higher critical charge during ionized particle strikes.

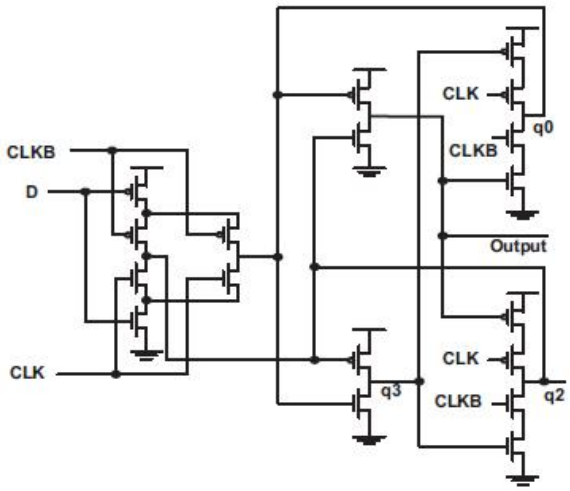

Fig 2.DICE Latch

Fig. 2illustrates the schematic of the DICElatch. The basic structure of the DICE latch includes two crosscoupledlatches, which are designed to inter-lock each other to astable logic state. The advantage of the DICE latch is that it has twostored logic value pairs, which are stored in q0, q1, and q2, q3.When a charge particle hits any single internal node, the node caneasily be recovered by the other three nodes. Therefore, DICE latchcan perform with better restoring capability. Even when upsetfaults occur on a

storage node and its complementary node (e.g.q3:0-1; q2:1-0), the logic values stored in the other two storagenodes (q1=0;q0=1) will remain correct.

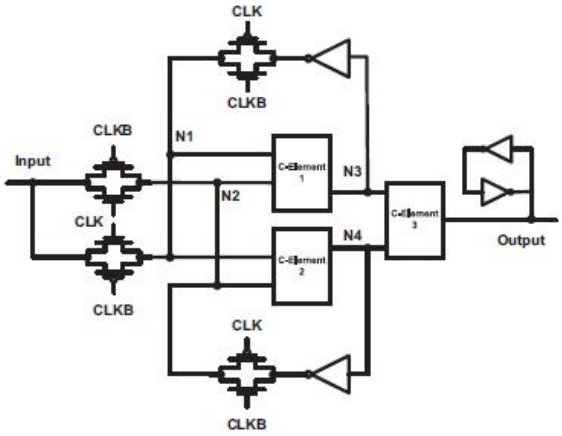

Fig 3.FERST Latch

Fig. 3 shows the FERST design [2] which exploits three C elements and two parallel latches to mask the propagation of soft error faults. As shown in Fig. 7, the C-element [2], [17], [18] has a unique property where the output node updates its logic state
only when the two input signals are identical. If the two inputs are different, the output remains at its previous state.

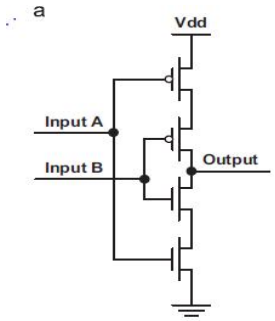

Fig4.C element

The FERST circuit uses three different C-elements to isolate the SEUs. For example, the C-elements 1 and 2 are used to prevent the transient fault of node N1 and N2 to propagate to the output. C-element 3 protects the output from the transient fault that occurs in nodes N3 and N4. When a charge hits any node, FERST latch can completely mask SEUs to prevent probable SEU faults on the output signal. The advantage of FERST latch is its superior SEUtolerance; however, its drawbacks arelarge power-delay-product and complicated hardware overhead.

Among the existing designs, the DICE latch can resist SEUs with lower hardware cost in terms of transistor count. However, DICE design still need to pay heavy hardware overhead to achieve superior SEU-tolerance since its transistor size should be increased to meet the demand for soft error resistance. FERST latch can provide superior SEU-tolerance. Generally speaking, the performance overhead in terms of power-delay product in the FERST design is lower than that in the DICE design while they achieve the same superior soft-error tolerance. In this paper, we will further present a SEU-tolerant latch with the same superior SEU-tolerant ability as FERST design but performs with lower PDP, which will be discussed in detail in the next section.

IMPROVED SEU-TOLERANT LATCH CIRCUIT

As shown in fig5the proposed Iso-DICE latch is designedbased on the DICE latch design and added with isolation mechanism. As illustrated , it is a positive level sensitive latch andits isolation mechanism is constructed by part 1, part 2, and part 3.The two additional MOS transistors, mpck and mnck, are utilizedto isolate node q1 apart from the output node to maintain itsstored logic state. When CLK=0 and CLK=1, the signal transmissionpaths from w3 and w4 to q1 are broken off. In this way, the logic state in the output node q1 can be protected and the impactof soft errors in the latch circuit can be suppressed. A feedback circuit is also utilized to maintain the logic state inw3 and w4. As a result, the high impedance

and the floating situation in nodes of w3 and w4 can all be avoided. In order toenhance the ability to resist soft errors and avoid the single eventupset from destroying the isolation mechanism, we set the logic state of w3 and w4 to be the inverse of q1 through this feedbackcircuit. In the latching mode, when output q1 is at logic '1', mpc2becomes off, mnc2 becomes on, and the nodes w3 and w4 are connected to the ground voltage level of VSS. Even when a SEUfrom logic '0' to logic '1' occurs in w3 and w4, the voltage of theoutput node is not affected. In the same way as output q1 is logic '0' in the latching mode, mnc2 becomes off, mpc2 becomes on, andthe nodes w3 and w4 are connected to the supply voltage level ofVDD instead. Moreover, in part 1 of the circuit, we connect the source terminals of mp3 and mn3 to CLK and CLKB respectively, whichcan prevent the latch from steady leakage during the latching mode.

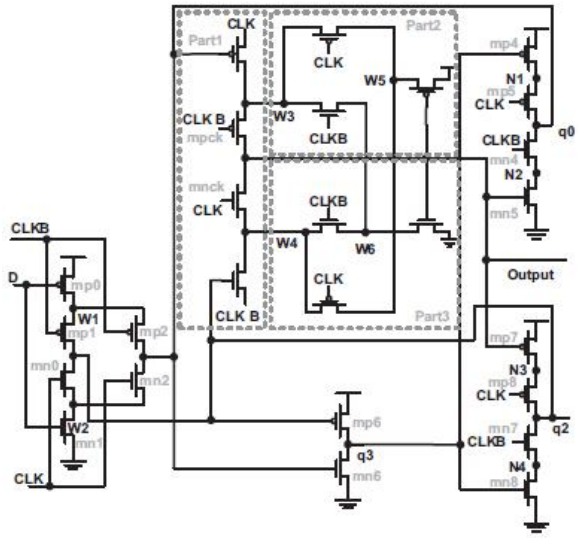

Fig 5.The Proposed Iso-DICE latch.

As illustrated in Fig. 6, in the latching mode if the logic statestored in q1 is '1', the transistors mnc2, mnc1, and mp3 all are on.The logic states of w3 and w6 all are '0', and the logic state of CLKis also '0' in the latching mode. As a result, the voltage level in theconducting path through CLK to w3 to w6 and VSS are all thesame. Therefore, there will be no steady current path existing.

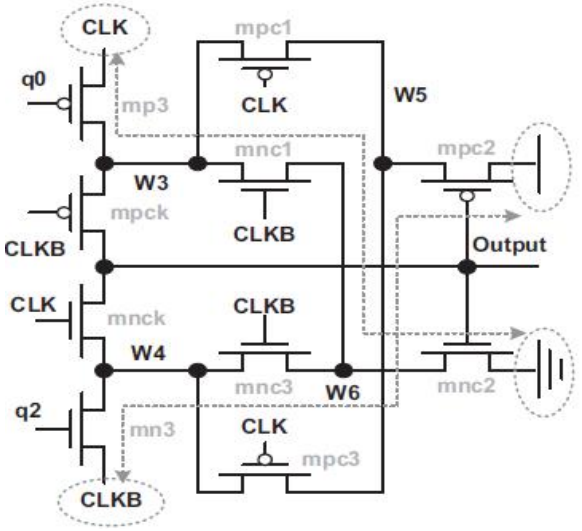

Fig 6.The steady current path can be removed and the SEU interference can beavoided in the latching mode of the proposed Iso-DICE latch.

Similarly, in the latching mode if the logic state stored in q1 is '0',the transistors mpc2, mpc3, and mn3 all are on. The logic states ofw4 and w5 all are '1', and the logic state of CLKB is also '1' in the

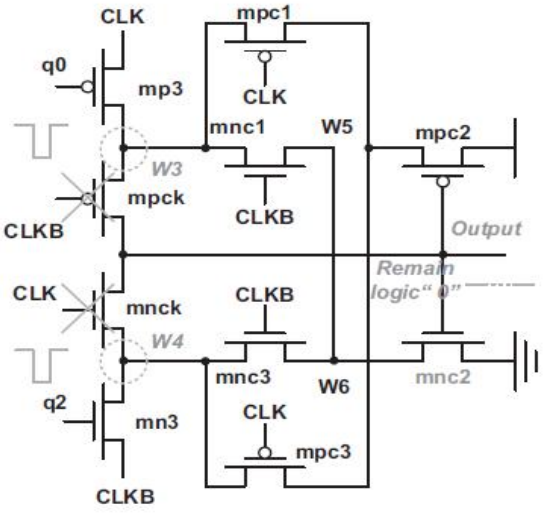

Fig 7.

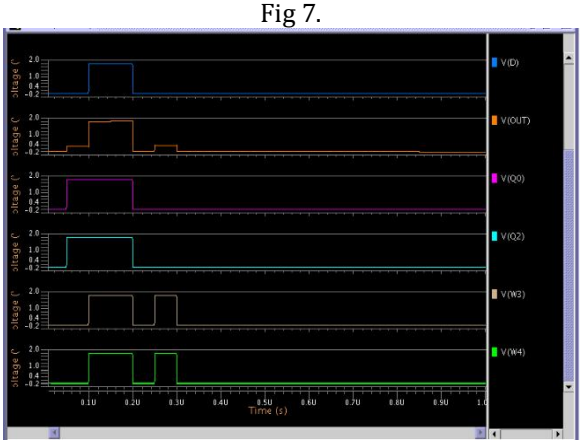

Fig 8.Output of the Proposed Iso-DICE latch.

latching mode. The voltage level in the conducting path throughCLKB to w4 to w5 and VDD are all the same. Therefore, there willbe no steady current path existing in the situation as q1 is '0', too.So, we can successfully prevent SEU's occurring in any internal
node from changing the logic state of the output node of the latch. Generally speaking, the function of Iso-DICE latch and DICElatch is similar in the transparent mode. However, when the latchis in its latching mode, DICE latch may suffer from soft error
interference if the particle energy is high enough. As for the latching mode of the proposed Iso-DICE latch, we can still resisthigh energy particle strikes because we construct the isolation mechanism between q1 and q0, q2. In the proposed Iso-DICE latchdesign, the circuit of part1 behaves as a CLK/CLKB controlled inverter, which can isolate the output node q1 apart from q0and q2 and protect it from being affected by faults occurring in the input node. The circuit of part 2 and part 3 are adopted to solve the floating problem of w3 and w4 and to preset the logic state of w3and w4 to be the complementary logic state of the output terminal
q1. As illustrated, even when the logic state in nodes w3and w4 is flipped by an ionized particle, a SEU just lets the logic level in nodes w3 and w4 flip into the same logic level as q1.Consequently, if any SEU occurs in the internal nodes of our proposed Iso-DICE latch, the output node q1 can always retainits stored logic value. The isolation mechanism constructed bycircuits of part 1, part 2, and part 3 enables the latch's output nodeto have high SEU tolerance when an ionized particle hits the
proposed Iso-DICE latch.
Because of the isolation property, the proposed Iso-DICE latch not only can resist single particle strike, but can also tolerate multiple soft error upsets. In addition to providing superior SEU-tolerant ability, the proposed Iso-DICE latch can perform with lower PDP. The keyreason to achieve such superior property is the adoption of isolation mechanism. In terms of power consumption comparison,

the DICE latch, the FERST latch, and the Iso-DICE latch all have nostatic power consumption. The FERST latch has a greater numberof switching transistors corresponding to the input transition and
it also consumes larger short circuit power. However, the DICElatch and the Iso-DICE latch cut down the probable short circuitleakage current path by turning-off mp5, mn4, mp6, and mn7when the clock signal is '1'. Thus the DICE latch and the proposed
Iso-DICE latch are able to consume lower dynamic power and lower short circuit power than the FERST latch. In regard of circuit operation delay time in the latch circuits, the difference comes because of signal transition stages and the number of cascaded MOS transistors causing the FERST latch to have a longer delaytime than that of the DICE latch. The proposed Iso-DICE latch alsohas longer delay time compared with the DICE latch due to theextra added MOS transistors applied to isolate soft errors. However,the proposed Iso-DICE design can resist SEU interferencethrough isolation mechanism, which need not increase the transistors size to raise their critical charge. Therefore, under the samesituation with superior SEU-tolerance, our proposed Iso-DICEdesign can perform with lowest PDP as compared with the state of-art of DICE [1] and FERST [2] designs.

RESULTS

Table 1:Comparison of Latches

Latch	Power	Delay
Dice	13.7288mW	50.140nS
Interdice	3.2583mW	438.05pS
Ferst	10.2975mW	99.677nS
Proposed Isodice	5.7833mW	50.511nS

Table 1 shows the comparison of different latches and their power and delay Here,the different latches were compared.Even though Ferst lowest power compared to dice latch power delay product of ferst latch is highest.In order to avoid that isodice latch circuit was proposed.it gives lower power and lower power delay product compared to dice and first latch.

CONCLUSION

In this paper, we proposed a robust SEU-tolerant latch design,which performs with lower PDP. Under TSMC 180 nm CMOS technology, experiment results show that both the Iso-DICE latchand the FERST latch have the capability of fully masking outputfaults caused by transient voltage in the internal nodes. However,the FERST latch consumes more energy and performs with largerPDP. Comparatively, the proposed Iso-DICE latch can perform withthe same superior SEU-immunity against soft errors as FERSTdesign, but performs with 55% lower PDP than FERST latch inTSMC 180 nm CMOS technology. As a result, the proposed Iso-DICE latch can provide both characteristics of low PDP and high capability of masking SEUs. Moreover,the proposed Iso-DICE latch can tolerate multiple nodes soft-errorupsets.

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